REMARKS

Claims 90 and 93-141 are pending in this application.

Claims 122, 125-129, 137, 140 and 141 stand rejected under 35 U.S.C. §102(b) as being anticipated by Rhodes (U.S. Patent No. 6,204,524) ("Rhodes"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a CMOS imager with improved charge storage. As such, independent claim 122 recites a "method of forming an imager" by *inter alia* " forming a photosensor including a charge collection region," "forming a floating diffusion region for receiving charge from said charge collection region" and "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected to said floating diffusion region by an electrical contact."

Independent claim 130 recites a "method of forming an imager" by *inter alia* "forming a field oxide region in said semiconductor substrate," "forming a photodiode in said doped layer" and "forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies said field oxide region." Independent claim 130 also recites "connecting an electrode of a charge storage capacitor to said photodiode by an electrical contact."

Independent claim 137 recites a "method of forming an imager" by *inter alia* "forming a photosensor including a charge collection region," "forming a floating diffusion region for receiving charge from said charge collection region" and "connecting an electrode of a first charge storage capacitor to said floating diffusion region by a first electrical contact." Independent claim 137 further recites "connecting an electrode of a second charge storage capacitor to said charge collection region by a second electrical contact."

Rhodes relates to a CMOS imager that "provides improved charge storage by fabricating a storage capacitor in parallel with the photocollection area of the imager." (Abstract). According to Rhodes, "[t]he storage capacitor may be a flat plate capacitor formed over the pixel, a stacked capacitor or a trench imager formed in the photosensor." (Abstract).

Rhodes fails to disclose all limitations of claims 122, 125-129, 137, 140 and 141. Rhodes does not disclose, teach or suggest "forming a floating diffusion region for receiving charge from said charge collection region" and "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected to said floating diffusion region by an electrical contact," as claim 122 recites. In Rhodes, storage capacitor 162, which would arguably correspond to the "charge storage capacitor" of the claimed invention, is connected to a fifth doped region 155 ("which is formed adjacent to the photogate 102") and not to the floating diffusion region 130. In addition, no electrode of the storage capacitor 162 of Rhodes is connected to a floating diffusion region "by an electrical contact," as in the claimed invention.

Rhodes is also silent about "forming a photodiode in [a] doped layer," "forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies said field oxide region" and "connecting an electrode of a charge storage capacitor to said photodiode by an electrical contact," as independent claim 130 recites. As described and illustrated in all figures of Rhodes, the trench and planar capacitor structures of Rhodes are all formed overlying the active area of the pixel sensor cell, and not such that "the entire extent of said charge storage capacitor overlies said field oxide region" (claim 130). Applicants also note that Figure 5 of Rhodes clearly shows parts of electrodes 156 and 160 of the capacitor 162 formed over the doped region 155 and the photogate 102 of the transistor 125 of Rhodes. Thus, storage

capacitor 162 of Rhodes is not illustrated in Figure 5 as "overl[ying] said field oxide region," as in the claimed invention.

Rhodes is also silent about "connecting an electrode of a first charge storage capacitor to [a] floating diffusion region by a first electrical contact," much less "connecting an electrode of a second charge storage capacitor to said charge collection region by a second electrical contact," as independent claim 137 recites. As noted above, Rhodes does not disclose, teach or suggest the step of connecting an electrode of a storage capacitor to a "floating diffusion region by a first electrical contact," as in the claimed invention. Rhodes is also silent about a "first charge storage capacitor" and a "second charge storage capacitor," much less about "connecting an electrode of a second charge storage capacitor to [a] charge collection region by a second electrical contact," as independent claim 137 recites. For at least these reasons, Rhodes fails to anticipate the subject matter of claims 122, 125-129, 137, 140 and 141, and withdrawal of the rejection of these claims is respectfully requested.

Claims 90, 93-101, 104-119, 123 and 130-136 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rhodes in view of Doyle et al. (U.S. Patent No. 6,300,662) ("Doyle"). This rejection is respectfully traversed.

As noted above, the claimed invention relates to a method of forming a CMOS imager with improved charge storage. As such, independent claim 90 recites a "method of forming a CMOS imager" by *inter alia* "providing a semiconductor substrate having a doped layer of a first conductivity type" and "forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region." Independent claim 90 also recites "forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies

said field oxide region" and "forming a contact between said first doped region and said charge storage capacitor."

Independent claim 108 recites a "method of forming a CMOS imager" by *inter alia* "providing a semiconductor substrate having a doped layer of a first conductivity type," "forming a field oxide region within said semiconductor substrate" and "forming a first conductive layer over said field oxide region and said substrate." Independent claim 108 also recites "forming an insulating layer over said first conductive layer," "forming a second conductive layer over said insulating layer" and "patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein the entire extent of said storage capacitor is formed over and in contact with said field oxide region."

Doyle relates to an "electronic programmable read-only-memory (EPROM) . . . having a field effect transistor with the gate electrode thereof coupled to a capacitor adapted to store charge produced in a channel region of the transistor in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode." (Abstract). Doyle teaches that "[t]he field effect transistor and the capacitor are formed in a common semiconductor body along with CMOS transistors." (Abstract).

The subject matter of claims 90, 93-101, 104-119, 123 and 130-136 would not have been obvious over Rhodes in view of Doyle. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference

teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, Rhodes and Doyle, whether considered alone or in combination, fail to disclose, teach or suggest all limitations of independent claims 90, 93-101, 104-119, 123 and 130-136.

Claims 90, 93-101 and 104-119

Rhodes and Doyle, alone or in combination, fail to disclose, teach or suggest all limitations of claims 90, 93-101 and 104-119. Rhodes does not disclose, teach or suggest "forming a charge storage capacitor such that *the entire extent of said charge storage capacitor overlies said field oxide region*" and "forming a contact between said first doped region and said charge storage capacitor," as independent claim 90 recites (emphasis added). Rhodes is also silent about "patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein *the entire extent of said storage capacitor is formed over and in contact with said field oxide region,*" as independent claim 108 recites (emphasis added).

Applicants submit that, as described and illustrated in all figures of Rhodes, the trench and planar capacitor structures of Rhodes are all formed overlying the active area of the pixel sensor cell, and not such that "the entire extent of said charge storage capacitor overlies said field oxide region" (claim 90) or "is formed over and in contact with said field oxide region" (claim 108). Applicants also note that the Abstract of Rhodes clearly specifies that "[t]he storage capacitor may be a flat plate capacitor *formed*

over the pixel, a stacked capacitor or a trench imager formed in the photosensor" (emphasis added), and not a capacitor the entire extent of which "overlies said field oxide region" or "is formed over and in contact with said field oxide region," as in the claimed invention. Applicants also note that Figure 5 of Rhodes clearly shows parts of electrodes 156 and 160 of the capacitor 162 formed over the doped region 155 and the photogate 102 of the transistor 125 of Rhodes. Thus, storage capacitor 162 of Rhodes is not illustrated in Figure 5 as "overl[ying] said field oxide region" or "formed over and in contact with said field oxide region," as in the claimed invention.

Similarly, Doyle is silent about a "method of forming a CMOS imager," much less about a "method of forming a CMOS imager" by "providing a semiconductor substrate having a doped layer of a first conductivity type," "forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region" and "forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies said field oxide region," as independent claim 90 recites. Doyle also fails to teach or suggest a "method of forming a CMOS imager," much less a "method of forming a CMOS imager" by the steps recited in independent claim 108.

Applicants also submit that, to establish a *prima facie* case of obviousness, "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a

determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573. This way, a rejection of a claim for obviousness in view of a combination of prior art references must be based on a showing of a suggestion, teaching, or motivation that has to be "clear and particular." In re Dembiczak, 175 F.3d at 999. Thus, the mere fact that it is possible to find two isolated disclosures which might be combined to produce a new compound does not necessarily render such production obvious, unless the prior art also suggests the desirability of the proposed combination.

The January 24, 2005 Office Action fails to establish a *prima facie* case of obviousness because, as the Court in Northern Telecom, Inc. noted, "[i]t is insufficient that the prior art disclosed the components of the patented device" and there is no "teaching, suggestion, or incentive to make the combination." Northern Telecom, Inc., 908 F.2d at 934. On one hand, the crux of Rhodes is the formation of a CMOS imager which comprises a storage capacitor formed in parallel with a photocollection area of the imager, to improve the signal-to-noise ratio and the dynamic range. Rhodes clearly emphasizes that "the storage capacitor [is] formed in parallel with a light sensitive node of the CMOS imager." (Col. 1, lines 7-10). On the other hand, the crux of Doyle is the formation of "programmable read-only-memories (EPROMs) . . . using sub-micron complementary metal oxide silicon (CMOS) processing techniques." (Col. 1, lines 8-10). Doyle emphasizes that "incorporation of an EPROM cell into a standard sub-micron CMOS process is difficult" because "[s]elf-aligned polycrystalline silicon floating and control gate electrodes . . . are not commonly used in CMOS processing" as "the channel length of the CMOS device is now less than a micron, control electrode voltages as low as 5 volts may result in 'hot' electrons being generated thereby requiring the CMOS devices to include lightly doped 'hot' electron suppression regions . . . to avoid high electric fields obtained with an abrupt drain-channel junction." (Col. 1,

lines 65-68; Col. 2, lines 1-12). Accordingly, a person of ordinary skill in the art would not have been motivated to combine Rhodes, which teaches formation of CMOS imagers and of a capacitor in parallel with a sensitive node of the CMOS imager, with Doyle, which teaches methods of suppressing the generation of "hot" electrons in EPROMs.

Claims 123 and 130-136

Rhodes and Doyle, alone or in combination, also fail to disclose, teach or suggest all limitations of claims 123 and 130-136. As noted above, Rhodes does not disclose, teach or suggest "forming a floating diffusion region for receiving charge from said charge collection region" and "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected to said floating diffusion region by an electrical contact," as independent claim 122 recites. Rhodes is also silent about a "method of forming an imager" by "forming a photodiode in [a] doped layer," "forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies said field oxide region" and "connecting an electrode of a charge storage capacitor to said photodiode by an electrical contact," as independent claim 130 recites. In Rhodes, storage capacitor 162, which would arguably correspond to the "charge storage capacitor" of the claimed invention, is connected to a fifth doped region 155 ("which is formed adjacent to the photogate 102") and not to the floating diffusion region 130. In addition, no electrode of the storage capacitor 162 of Rhodes is connected to a floating diffusion region "by an electrical contact," as in the claimed invention.

Similarly, Doyle is silent about a "method of forming a CMOS imager" or about a "method of forming an imager," much less about "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected to [a] floating

diffusion region by an electrical contact" (claim 122) or "connecting an electrode of a charge storage capacitor to [a] photodiode by an electrical contact" (claim 130). For at least these reasons, Applicants submit that the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 90, 93-101, 104-119, 123 and 130-136 is respectfully requested.

Claims 102, 103, 120 and 121 stand rejected under 35 U.S.C. §103 as being unpatentable over Rhodes in view of Doyle and further in view of Perner (U.S. Patent No. 6,262,703). This rejection is respectfully traversed.

Claims 102 and 103 depend on independent claim 90 and recite that the gate is "a gate of a global shutter transistor." Claims 120 and 121 depend on independent claim 108 and recite that the electrical element is "a gate of a global shutter transistor."

Perner relates to a "pixel within an array of pixels in which each pixel cell includes circuitry for generating its own DC balance data by utilizing the display data that is transferred to the pixel from an external source." (Abstract). According to Perner, "[e}ach pixel cell includes an initial storage node that branches into two separate storage nodes, the first of the branched nodes being used to store data that is used for display by the pixel and the second of the branched nodes being used to generate and hold the DC balance data." (Abstract).

As noted above, Rhodes and Doyle, alone or in combination, fail to disclose, teach or suggest all limitations of independent claims 90 and 108. Similarly, Perner is silent about any of the limitations of claims 90 and 108. Perner relates to a "method . . . for reducing data transfer requirements to a pixel cell involve an array of pixels in which each pixel cell includes circuitry for generating its own DC balance data," and not to methods of forming CMOS imagers, as in the claimed invention. Accordingly,

and for at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness. Withdrawal of the rejection of claims 102, 103, 120 and 121 is also respectfully requested.

Claims 124 and 139 stand rejected under 35 U.S.C. §103 as being unpatentable over Rhodes in view of Merrill et al. (U.S. Patent No. 6,741,283) ("Merrill"). This rejection is respectfully traversed.

Claim 124 depends on independent claim 122 and recites that "the entire extent of said charge storage capacitor overlies an active area of said photosensor." Claim 139 depends on independent claim 137 and recites that "a first portion of said first charge storage capacitor is formed over said field oxide region, and . . . a second portion of said first charge storage capacitor is formed over an active area of said photodiode."

Merrill relates to a "storage pixel sensor disposed on a semiconductor substrate compris[ing] a capacitive storage element having a first terminal connected to a fixed potential and a second terminal." (Abstract). Merrill teaches that "[a] photodiode has an anode connected to a first potential and a cathode" and that "[a] semiconductor reset switch has a first terminal connected to the cathode and a second terminal connected to a reset potential." (Abstract). Merrill also teaches that "[a] semiconductor transfer switch has a first terminal connected to the cathode and a second terminal connected to the second terminal of the capacitive storage element" and that "[a] semiconductor amplifier has an input connected to the capacitive storage element and an output." (Abstract).

Rhodes and Merrill, whether considered alone or in combination, fail to disclose, teach or suggest all limitations of claims 122 and 137. As noted above, Rhodes

does not disclose, teach or suggest "forming a floating diffusion region for receiving charge from said charge collection region" and "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected to said floating diffusion region by an electrical contact," as independent claim 122 recites. Rhodes also fails to teach or suggest "connecting an electrode of a first charge storage capacitor to [a] floating diffusion region by a first electrical contact," much less "connecting an electrode of a second charge storage capacitor to said charge collection region by a second electrical contact," as independent claim 137 recites. Similarly, Merrill is silent about any of the limitations of independent claims 122 and 137. Accordingly, and for at least the reasons above, the Office Action fails again to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 124 and 139 is also respectfully requested.

Claim 138 stands rejected under 35 U.S.C. §103 as being unpatentable over Rhodes in view of Fossum et al. (U.S. Patent No. 6,744,084) ("Fossum"). This rejection is respectfully traversed.

Applicants submit that the earliest effective filing date of the present application is November 26, 2002. Fossum was filed on August 29, 2002 and issued on June 1, 2004. Fossum thus qualifies as prior art only under 35 U.S.C. § 102(e). In addition, the subject matter of Fossum and of the claimed invention were, at the time the invention was made, subject to an obligation of assignment to the same entity: Micron Technology, Inc. The Assignment for this application was recorded in the Patent and Trademark Office on November 26, 2002 on Reel 013524, Frame 0415. The Assignee of Fossum is shown on the face of the reference. Therefore, section 35 U.S.C. § 103(c) applies. According to MPEP § 706.02(l)(1), "[e]ffective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is

now disqualified as prior art against the claimed invention if that subject matter and the claimed invention 'were, at the time the invention was made, . . . subject to an obligation of assignment to the same person.'" Accordingly, Fossum is not a valid prior art reference and should be excluded under 35 U.S.C. § 103.

Allowance of claims 90 and 93-141 is solicited.

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Respectfully submitted,

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